

REMARKS

Claims 1 through 10 are pending in this application. Claim 5 is being amended by this Amendment to correct typographical error.

The Examiner's withdrawal of the finality of the previous Office action and the re-opening of prosecution is noted with appreciation.

Claims 1 through 10 remain pending.

Claims 1, 2, 9 and 10 are newly rejected under 35 U.S.C. §103(a) as rendered obvious over a proposed combination of Miichi U.S. 5,880,745 modified according to Applicant's Cho U.S. 6,198,468. Applicant respectfully traverses this rejection for the following reasons.

Miichi '745 expressly reliance upon both the analog-to-digital converter 36 to convert the R G and B image signals into digital signals to be applied to signal converter 37 (see Miichi '745, column 8, lines 55 and 56) and phase-locked loop 40 to stabilize the signals in order to adjust the timing. (See Miichi '745, column 8, lines 66 and 67).

Cho '468 expressly incorporates a phase-locked loop 96, in conjunction with a mask signal generator 92 and an external horizontal synchronous signal generator 94 to "constitute video signal compensation portion 100" illustrated in Fig. 1.

As was previously explained to the Examiner, Applicant's specification describes

the circuit of Miichi '745 on page 2, lines 2 through 10, and identifies the difficulties with such circuit. These difficulties include a sampling operation "at a rate of at least twice the frequency of the analog video signal" received, and the necessity for the phase-locked loop to have a wide locking range, and a limitation upon the "allowable frequency range of the import signal" do to the operational characteristics of the analog-to-digital circuit and the phase-locked-loop.

Claim 1 expressly defines a novel circuit that provides a synchronizing signal and analog video signal to an analog display signal, without reliance upon either an analog-to-digital converter or a phase-locked loop for a signal conversion. Accordingly, the Examiner's proposed combination fails to make a *prima facie* showing of obviousness.

In essence, both Miichi '745 and Cho '486 require a phase-locked loop in order to generate a clock signal in response to the synchronizing signal receive from the host personal computer, as is described in an Applicant's background discussion and in both of these references, and therefore both suffer from the deficiencies noted in lines 11 through 18 of Applicant's background discussion presented upon page 2 of the specification. In contradistinction, claim 9 expressly defines a display apparatus "converting set data into a corresponding video signal without utilization of an analog-to-digital converter (ADC) or a phase-locked loop (PLL) circuit." Independent method claim 10 describes the generation of "a synchronizing signal by extracting the synchronizing data from set

reconstructed display information” in combination with “converting set video data into a corresponding signal without utilizing an analog-to-digital converter (ADC) or phase-locked loop (PLL) circuit.”

The Examiner’s assertion that “Cho teaches a first external horizontal signal generator (86) which generate the synchronous signal from [?] corresponding to the display mode” does nothing to remedy the deficiencies in the primary reference. In fact, the signal generator 86 of Cho ‘468 subsequently drives phase-locked loop 96, to provide video signal compensation, as is expressly explained in column 3, lines 30 through 34 of Cho ‘468. Therefore, the Examiner’s proposed combination fails to satisfy all of the limitation in characteristics of the subject matter defined by rejected claims 1, 2, 9 and 10. Moreover, the Examiner’s proposed combination fails to provide the remedy for the deficiencies noted in lines 11 through 18 on page 2 of Applicant’s specification. The fact that Applicant alone both recognizes these deficiencies attributable to use of the analog-digital converter and phase-locked-loop, is itself convincing indicia of the non obviousness of the subject matter defined by these claims. Accordingly, withdraw of this rejection is required.

Claims 3 through 8 were rejected under 35 U.S.C. §103 as rendered obvious over proposed combination of Miichi ‘745 modified according to Rokunohe U.S. 4,549,175. Applicant respectfully traverses this rejection for the following reasons.

In support of the rejection the Examiner asserts that Rokunohe '175 provides a flat panel display with means "for connecting to an analog display." Rokunohe '175 however, expressly requires "A/D/B converter 12 [that] serves to convert the analog RGB electric signals ... into corresponding RGB signals in 64 levels (6 bits) of shade for each picture element (.) of one scene." (Column 3, lines 30-35). In short, although Rokunohe '175 may in fact provide an analog display Rokunohe '175 fails to remedy the deficiencies noted in the foregoing paragraphs in the primarily reference. Independent apparatus claim 3, together with claim 6 through 8 depending thereon, expressly define Applicant's system as not utilizing "any analog-to-digital converter (ADC) or phase-locked-loop (PLL) circuit for signal conversion. The Examiner's proposed combination including Rokunohe '175 inherently use this both, and consequently suffers from the deficiencies noted in lines 11 through 18 on page 2 of Applicant's background discussion.

The fact that the Examiner's proposed combination neither recognized nor addressed these deficiencies, this further indicia of the obviousness *vel non* of claims 3 and 6 through 8.


Moreover, the Examiner's proposed combination does nothing to remove the deficiencies in the primary reference noted in a foregoing paragraphs; consequently, claims 4 and 5 which ultimately depend upon parent claim 1, are patenatably distinguishable and allowable over the Examiner's proposed combination.

Applicant notes, in an overall observation, that is extremely difficult to understand the Examiner's reliance upon three references which are generally discussed in the Applicant's background discussion, particularly one Applicant has undertaken the effort to identify the deficiencies in references such as these, and to also identify the source of those difficulties. The fact that the pending claims expressly exclude the circuits defined by these references, should clearly indicate to the Examiner's patentable distinction of the pending claims over these exemplars of art. Accordingly, there is no further basis for maintaining these rejections, and both rejection should be withdrawn.

In view of the above, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Reconsideration of the rejections and objections is requested. Should any questions remain unresolved, the Examiner is requested to telephone Applicant's attorney.

No fees are incurred by this response.

Respectfully submitted,



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MARKED-UP VERSION OF AMENDMENT

IN THE SPECIFICATION

Please enter the following amendments:

1. Please amend the first complete paragraph on page 2 (page 2, lines 2-10) as follows:

An LCD system generally includes an ADC (Analog-to-Digital Converter), a PLL circuit (Phase Locked Loop), a video data converter, an LCD driver, and an LCD panel [the] . The ADC converts an analog R(red), G(green) and B(blue) video signal to corresponding digital video data. The PLL circuit generates an internal clock signal in response to a synchronizing signal received from a host. The video data converter converts the digital video data according to a clock signal. This is to accommodate the dot and line numbers of the video data supplied to the LCD driver when the resolution provided by the host differs from that of the display. The LCD panel is driven by the LCD driver, displaying the video signal. Such a flat panel display systemsuffers from the following drawbacks:

2. Please amend the first paragraph on page 4 (page 4, lines 1-7) as follows:

According to an embodiment of the present invention, a flat panel display for receiving display information including video data and synchronizing data from a host processing digital data in a serial digital communication, [comprises:] may be constructed with a receiver for reconstructing the display information, a synchronizing signal generator for generating a synchronizing signal by extracting the synchronizing data from the reconstructed display information, a digital-to-analog converter (DAC) for converting the video data to a corresponding video signal, and an output terminal for externally transferring the synchronizing signal and analog video signal to an analog display.

3. Please amend the third paragraph on page 4 (page 4, lines 12-20) as follows:

According to another embodiment of the present invention, there is provided a digital data processing device, which may be used in a flat panel display for displaying display information received from a host processing digital data, and [comprises:] a transmitter connected to the host to transfer digital display information [in] as serial data, a receiver for reconstructing the display information, a synchronizing signal generator for

generating a synchronizing signal by extracting the synchronizing data from the reconstructed display information, a DAC for converting the video data to a corresponding video signal, and an output terminal for externally transferring the synchronizing signal and analog video signal to an analog display. The flat panel display includes the receiver, synchronizing signal generator and output terminal.

IN THE CLAIMS

Please amend claim 5, as follows:

1 5 (amended twice). The display apparatus of claim 1, said analog display
2 apparatus comprising:

3 an amplifier for receiving said video signal from said DAC via said output
4 terminal and amplifying said video signal;

5 a deflection signal generator for receiving said synchronizing signal output from
6 [aid] said synchronizing signal generator via said output terminal and for
7 generating deflection signals;

8 a high voltage generator for receiving an output from said deflection signal
9 generator and generating a high voltage;

10 a cathode ray tube (CRT) display for receiving said amplified video signal from
11 said amplifier and output signals from said deflection signal generator and a
12 high voltage from said high voltage generator.